

1 WHAT IS CLAIMED IS:

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3 1. A programmable, single chip embedded processor system for
4 input/output applications, comprising:

5 a modular, multiple bit, multithread processor core operable
6 by at least four parallel and independent application threads
7 sharing common execution logic segmented into a multiple
8 stage processor pipeline, wherein said processor core is
9 capable of having at least two states;

10 a logic mechanism engaged with said processor core for executing
11 an instruction set within said processor core;

12 a supervisory control unit, controlled by at least one of
13 said processor core threads, for examining said core
14 processor state and for controlling said core processor
15 operation;

16 a memory for storing and executing said instruction set data;
17 and

18 a peripheral adaptor engaged with said processor core for
19 transmitting input/output signals to and from said processor
20 core.

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22 2. A system as recited in Claim 1, wherein said processor
23 pipeline includes an instruction fetch logic stage, instruction
24 decode logic stage, multiple port register read stage, address
25 mode logic stage, arithmetic logic unit for arithmetic and address
26 calculations stage, multiple port memory stage, branch/wait logic
27 stage and multiple port register write stage.

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29 3. A system as recited in Claim 1, wherein said processor core
30 supports "n" multiple groups of independent threads by replicating
31 said common execution logic and said memory.

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33 4. A system as recited in Claim 1, further comprising a
34 condition code mechanism implemented in said instruction set for
35 detecting specific word data types.

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37 5. A system as recited in Claim 4, wherein the value of the
38 least significant byte of a word is detected to be within a
39 specific range.

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41 6. A system as recited in Claim 1, wherein said instruction set
42 includes a processor instruction for enabling individual threads
43 to determine their thread identity.

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45 7. A system as recited in Claim 1, wherein said supervisory
46 control unit is capable of examining and interpreting the state of
47 multithread processor core operation for the purpose of starting,
48 stopping, and modifying individual multithread processor
49 operation.

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51 8. A system as recited in Claim 7, further comprising a
52 hardware semaphore vector engaged with said supervisory
53 control unit for controlling multithread access to said peripheral
54 and system memory.

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56 9. A system as recited in Claim 1, wherein said supervisory
57 control unit is capable of being accessed and controlled by each
58 of said operating core processor threads by using input/output
59 instructions.

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61 10. A system as recited in Claim 9, wherein said controlling
62 operating processor thread is programmable and comprises any of
63 the available threads.

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65 11. A system as recited in Claim 9, wherein said controlling
66 operating core processor thread is capable of reconfiguring the
67 overall thread processing method of operation so that other
68 processing threads can support multiple instruction multiple data
69 processing operations.

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71 12. A system as recited in Claim 9, wherein said controlling
72 operating processor thread can reconfigure the overall thread
73 processing method of operation so that other processing threads
74 can support single instruction multiple data processing
75 operations.

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77 13. A system as recited in Claim 9, wherein said controlling
78 operating processor thread is capable of reconfiguring the overall
79 thread processing method of operation so that an arbitrary number
80 of processing threads can support simultaneously single
81 instruction multiple data processing operations and multiple
82 instruction multiple data processing operations.

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84 14. A system as recited in Claim 1, wherein said supervisory
85 control unit is operable by a first thread process to start and
86 stop another thread process and to examine and alter state
87 information in single step and multiple step modes of controlled
88 operation.

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90 15. A system as recited in Claim 1, further comprising
91 identifying bit patterns embedded in the unassigned bit fields of
92 the machine instructions of said core processor.

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94 16. A system as recited in Claim 1, wherein said memory
95 comprises internal memory for storing and executing core processor
96 code and external memory engaged with said peripheral adaptor.

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98 17. A system as recited in Claim 1, wherein said supervisory
99 control unit is configured as a peripheral to said processor core.

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101 18. A system as recited in Claim 1, wherein said peripheral
102 adaptor is capable of controlling analog and digital processing
103 functions.

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